R5640G Series

2 to 5 Serial Cell Li-ion Battery Protection IC for Secondary Protection

NO.EA-425-250728

OVERVIEW

The R5640G is an overcharge protection IC for 2- to 5- series cell Li-ion / Li-polymer rechargeable battery pack, with built-in high-accuracy voltage detection circuits and delay circuits. Controlling the supply voltage to the CTLC pin can control the COUT pin output. The shutdown detection can reduce the supply current to the minimum.

KEY BENEFITS

- Reducing the supply current to 0.2 μA or less after shutdown detection can achieve the longer battery life.
- Cascading the R5640G of 2 or more is adaptable to the battery pack of 6 or more cells and results in a reduction of external parts.
- Be adaptable to 30 V input voltage by using high-voltage process.

KEY SPECIFICATIONS

- Overcharge Detection Voltage(V_{DET1n}[(1)]): 2.90 V to 4.70 V (5 mV step)
- Overcharge Detection Voltage Accuracy: ± 0.016 V (Ta = 25°C)
  ± 0.025 V (0°C < Ta < 60°C)
- Overcharge Release Voltage(V_{REL1n}[(1)]):
  V_{DET1n} -0V[(2)] to V_{DET1n} -0.4V (V_{DET1}≥3.0V, 50 mV step) /
  V_{DET1n} -0V[(2)] to V_{DET1n} -0.35V(V_{DET1}<3.0V, 50 mV step)
- Overcharge Detection Delay Time: 2 / 4 / 6 / 10 / 16 sec
- Release Condition: Voltage Release Type
- Low Supply Current: Typ.2.5 μA
- Shutdown Current: Max. 0.2 μA
- Shutdown Detection Voltage: Typ. 2.1V±0.3V / 2.5V±0.3V / 3.7V±0.3V
- 2 to 5 Cells Selectable Battery Protection by External Wirings
- Selectable Timer Reset Delay Function
- Available Cascade Connection
- CTLC Pin Detection Delay Time: 2 msec
- Output Type: Pch. Open-drain of Internal Regulator

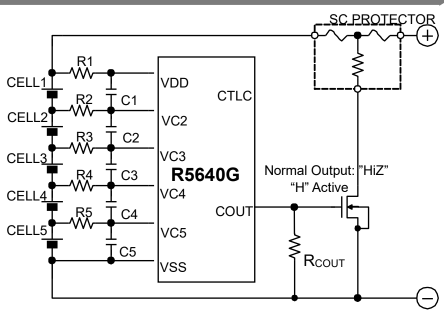
OPTIONAL FUNCTIONS

User-selectable Delay Time and Timer Reset Delay Function:

Code ($)	Overcharge Detection Delay Time
A	2 sec
B	4 sec
C	6 sec
D	10 sec
E	16 sec

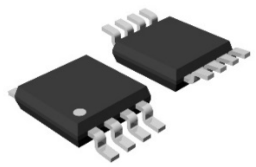
Code (*)	Timer Reset Delay Function
A	Disable
B	Enable

TYPICAL APPLICATION CIRCUIT



Typical Application Circuits for 5 Cells Protection

PACKAGE



MSOP-8

3.0 mm x 4.9 mm x 0.85 mm

APPLICATIONS

- Li-Ion or Li-Polymer Battery Protection

(1) V_{DET1n}, V_{REL1n} : n =1, 2, 3, 4, 5
(2) Min. 4.05 V when shutdown detection voltage (V_{SHTn}) is 3.7 V.

SELECTION GUIDE

Overcharge detection / release voltages and delay time are user-selectable options.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5640Gxxx$∗-E2-FE	MSOP-8	3,000	Yes	Yes

xxx: Specify the combination of the overcharge detection voltage (V_{DET1n}), the overcharge release voltage (V_{REL1n}), and the shutdown detection voltage (V_{SHTn}).

V_{DET1n}[1] : 2.9 V to 4.7 V in 5 mV step

V_{REL1n}[1]: V_{DET1n}-0V[2] to V_{DET1n}-0.4V (V_{DET1}≥3.0V) / V_{DET1n}-0V[2] to V_{DET1n}-0.35V(V_{DET1}<3.0V) in 50 mV step

V_{SHTn}[1] : 2.1V / 2.5V / 3.7 V

$: Specify the delay time code defined a combination of the overcharge detection delay time (t_{VDET1}), the overcharge release delay time (t_{VREL1}), and the CTLC detection delay time (t_{CDET}).

Code	t_{VDET1} (s)	t_{VREL1} (ms)	t_{CDET} (ms)
A	2	16.5	2
B	4	16.5	2
C	6	16.5	2
D	10	16.5	2
E	16	16.5	2

∗: Specify the timer reset delay function.

Code	Timer Reset Delay Function
A	Disable
B	Enable

[1] V_{DET1n}, V_{REL1n}, V_{SHTn}: n =1, 2, 3, 4, 5

[2] Min. 4.05 V when shutdown detection voltage (V_{SHTn}) is 3.7 V.

Product Code List

The product code is determined by the combination of the set output voltage (overcharge detector threshold: V_{DET1n}, overcharge release voltage: V_{REL1n}, shutdown detector threshold: V_{SHTn}) and the delay time (overcharge detection delay time: t_{VDET1}, overcharge release delay time: t_{VREL1}, CTLC detection delay time: t_{CDET}) and the timer reset delay time option (t_{VTR}).

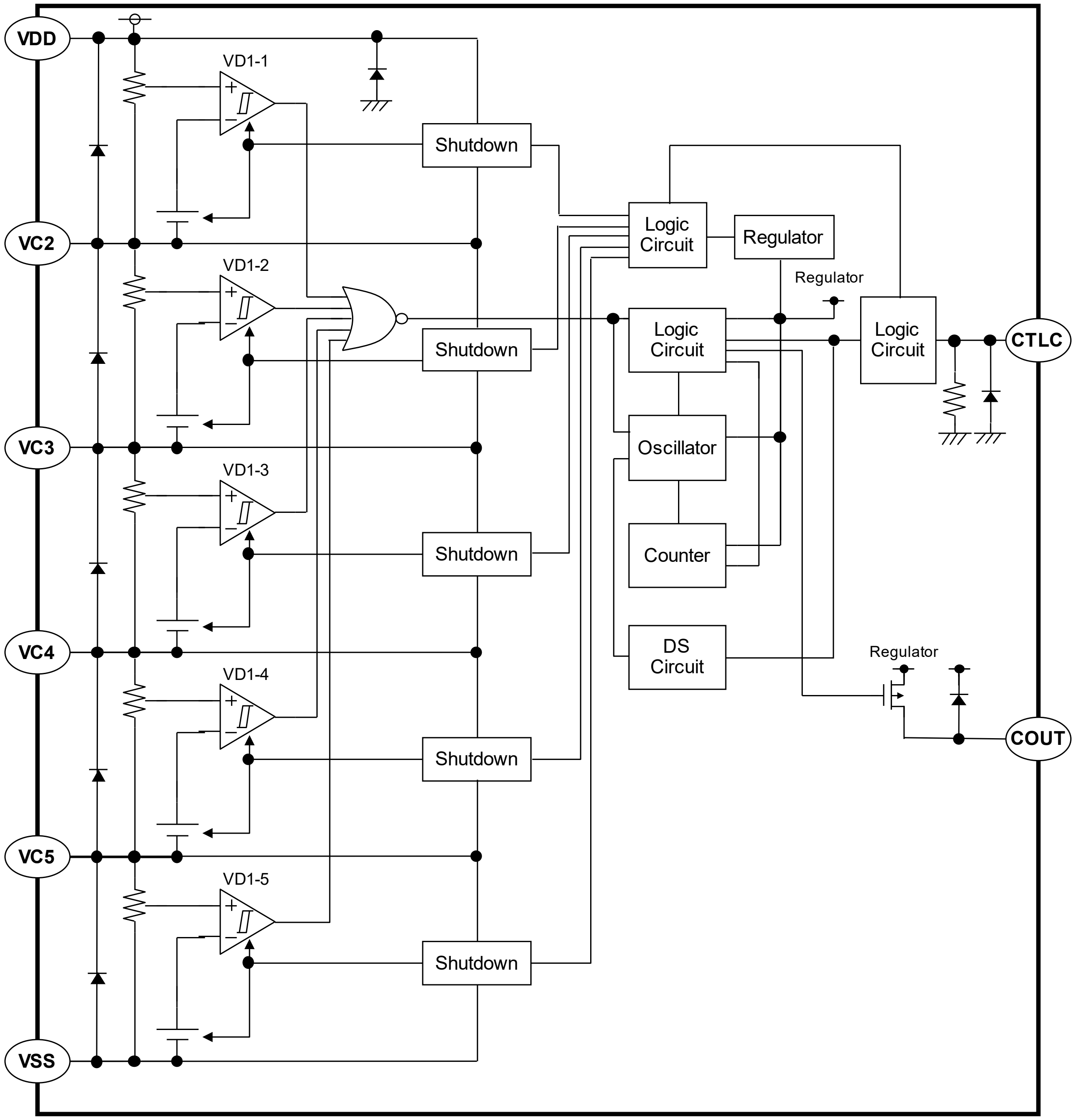
Product Code Table

Product Name	Set Output Voltage [V]			Delay Time			Timer Reset Delay Time (Yes/No[1])
	V_{DET1n}	V_{REL1n}	V_{SHTn}	t_{VDET1} [s]	t_{VREL1} [ms]	t_{CDET} [ms]	
R5640G251DA	4.220	4.050	3.700	10	16.5	2	No
R5640G252AB	4.220	4.120	3.700	2	16.5	2	Yes
R5640G301BA	4.300	4.000	2.500	4	16.5	2	No
R5640G302BA	4.350	4.050	2.500	4	16.5	2	No
R5640G305BB	4.300	3.900	2.500	4	16.5	2	Yes
R5640G101BB	3.750	3.450	2.500	4	16.5	2	Yes
R5640G254AB	4.200	4.100	3.700	2	16.5	2	Yes
R5640G471AA	2.900	2.700	2.100	2	16.5	2	No
R5640G472AA	3.000	2.800	2.100	2	16.5	2	No
R5640G256AB	4.275	4.100	3.700	2	16.5	2	Yes
R5640G302DA	4.350	4.050	2.500	10	16.5	2	No
R5640G102AA	3.900	3.700	2.500	2	16.5	2	No
R5640G352BA	4.175	4.050	3.700	4	16.5	2	No

Please contact our sales representatives if required a product code other than the above combinations.

[1] “No” means the timer reset delay time option is absent.

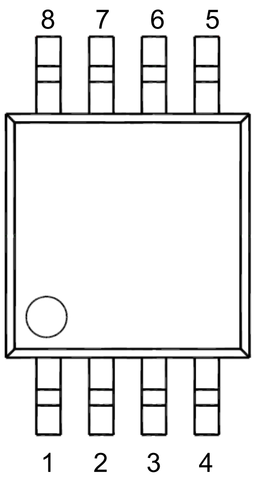
BLOCK DIAGRAM



R5640G Block Diagram

PIN DESCRIPTION

Top View



MSOP-8 Pin Configuration

R5640G Pin Description

Pin No.	Symbol	Description
1	VDD	Power Supply Pin, Positive Terminal for CELL1
2	VC2	Positive Terminal for CELL2
3	VC3	Positive Terminal for CELL3
4	VC4	Positive Terminal for CELL4
5	VC5	Positive Terminal for CELL5
6	VSS	Ground Pin
7	CTLC	COUT Control Pin / Output Delay Time Shortening Pin
8	COUT	Overcharge Detection Output Pin, Pch. Open-drain Output

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C, V_{SS} = 0V)

Symbol	Item	Ratings	Unit
V_{DD}	Supply Voltage (Positive Terminal Voltage for CELL1)	-0.3 to 30 V_{C2}-0.3 to V_{C2}+6.5	V V
V_{C2}	Positive Terminal Voltage for CELL2	V_{C3}-0.3 to V_{C3}+6.5	V
V_{C3}	Positive Terminal Voltage for CELL3	V_{C4}-0.3 to V_{C4}+6.5	V
V_{C4}	Positive Terminal Voltage for CELL4	V_{C5}-0.3 to V_{C5}+6.5	V
V_{C5}	Positive Terminal Voltage for CELL5	-0.3 to 6.5	V
V_{CTLC}	CTLC Pin Voltage	-0.3 to 30	V
V_{COUT}	COUT Pin Output Voltage	V_{OH1}-30 to V_{OH1}+0.3	V
P_D	Power Dissipation (MSOP-8, JEDEC STD.51-7)	960	mW
Tj	Junction Temperature Range	-40 to 125	°C
Tstg	Storage Temperature Range	-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITION

Symbol	Item	Rating	Unit
V_{DD}	Operating Input Voltage	4.0 to 25 / V_{C2}+5 V	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

V_{CELLn} = CELLn (Ex. V_{CELL1} is a voltage difference between VDD and VC2), n = 1, 2, 3, 4, 5, unless otherwise noted. The specifications surrounded by ☐ are guaranteed by Design Engineering at 0°C ≤ Ta ≤ 60°C.

(Ta = 25°C)

Symbol	Parameter	Conditions	Ratings Min.	Ratings Typ.	Ratings Max.	Unit	Circuit [1]
V_{DET1n}	CELLn overcharge detection voltage	at rising edge of voltage	V_{DET1n} -0.016V V_{DET1n} -0.025V	V_{DET1n}	V_{DET1n} +0.016V V_{DET1n} +0.025V	V	A
V_{REL1n}	CELLn overcharge release voltage	at falling edge of voltage	V_{REL1n} -0.050V	V_{REL1n}	V_{REL1n} +0.050V	V	A
t_{VDET1}	Overcharge detection delay time	V_{CELLn}=V_{DET1n}-0.1V (n=2,3,4,5) V_{CELL1} = V_{DET1n}-0.1V → 4.7 V ($V_{DET1n} \leq$ 4.6 V) or → 4.8V (V_{DET1n} > 4.6V)	t_{VDET1} x 0.8	t_{VDET1}	t_{VDET1} x 1.2	s	B
t_{VD1DS}	Overcharge detection delay time at delay shortening mode	V_{CELLn}=V_{DET1n}-0.1V (n=2,3,4,5) V_{CELL1} = V_{DET1n}-0.1V → 4.7 V ($V_{DET1n} \leq$ 4.6V) or → 4.8V (V_{DET1n} > 4.6V) V_{CTLC} = 2.0V	0.5	4	8	ms	B
t_{VREL1}	Overcharge release delay time	V_{CELLn}=V_{REL1n}-0.1V (n=2,3,4,5) V_{CELL1} = 4.7 V ($V_{DET1n} \leq$ 4.6 V) or 4.8V (V_{DET1n} > 4.6V) → V_{REL1n}-0.1V	t_{VREL1} x 0.8	t_{VREL1}	t_{VREL1} x 1.2	ms	B
t_{VTR}	Overcharge detection timer reset delay time [2]	V_{CELLn}= V_{DET1n}+0.05 V → V_{REL1n}-0.10 V → V_{DET1n}+0.05 V → V_{REL1n}-0.10 V	2	6	10	ms	B
V_{SHTn}	Shutdown detection voltage	at falling edge of voltage	V_{SHTn} -0.3V	V_{SHTn}	V_{SHTn} +0.3V	V	C
V_{IH}	CTLC pin input voltage, high		2.8			V	D
V_{IM}	CTLC pin input voltage, middle		1.9		2.4	V	D
t_{CDET}	CTLC pin detection delay time	V_{CELLn}=V_{DET1n}-0.1V V_{CTLC}=0.0V→3.0V	t_{CDET} x 0.8	t_{CDET}	t_{CDET} x 1.2	ms	D
		V_{CELLn}=V_{SHTn}-0.4V V_{CTLC}=0.0V→3.0V(at shutdown)		t_{CDET}+1			
I_{CTLC}	CTLC pin current	V_{CELLn}=V_{DET1n}-0.1V, V_{CTLC}=3.0V	0.13	0.3	0.55	μA	D
I_{LCOUT}	COUT pin off-leakage current	V_{CELLn}=V_{DET1n}-0.1V V_{COUT}=-10.0V	-0.1			μA	E

(1) Refer to *TEST CIRCUITS* for detail information.
(2) For the timer reset delay function enabled product only

V_{CELLn} = CELLn (Ex. V_{CELL1} is a voltage difference between VDD and VC2), n = 1, 2, 3, 4, 5, unless otherwise noted. The specifications surrounded by ☐ are guaranteed by Design Engineering at 0°C ≤ Ta ≤ 60°C.

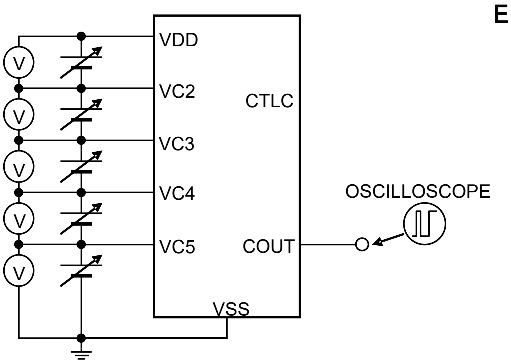
(Ta = 25°C)

Symbol	Parameter	Conditions	Ratings			Unit	Circuit (1)
V_{OH1}	COUT pin Pch. ON voltage1	I_{OH}= -1μA, V_{CELLn} = 4.7 V (V_{DET1n} ≤ 4.6 V) or 4.8V (V_{DET1n} > 4.6V)	4.0	4.7	5.4	V	F
V_{OH2}	COUT pin Pch. ON voltage2	I_{OH}= -50 μA, V_{CELLn} = 4.7 V (V_{DET1n} ≤ 4.6 V) or 4.8V (V_{DET1n} > 4.6V)	V_{OH1} -0.5V	V_{OH1} -0.11V		V	G
I_{SHT}	Shutdown current	V_{CELLn} = V_{SHTn}-0.4 V			0.2	μA	H
I_{SS}	Supply Current	V_{CELLn} = V_{DET1n}-0.1V		2.5	5.0	μA	H
I_{VC2}	VC2 pin current	V_{CELLn} = V_{DET1n}-0.1V	-0.3		0.3	μA	H
I_{VC3}	VC3 pin current	V_{CELLn} = V_{DET1n}-0.1V	-0.3		0.3	μA	H
I_{VC4}	VC4 pin current	V_{CELLn} = V_{DET1n}-0.1V	-0.3		0.3	μA	H
I_{VC5}	VC5 pin current	V_{CELLn} = V_{DET1n}-0.1V	-0.3		0.3	μA	H

(1) Refer to *TEST CIRCUITS* for detail information.

Test Circuits

A



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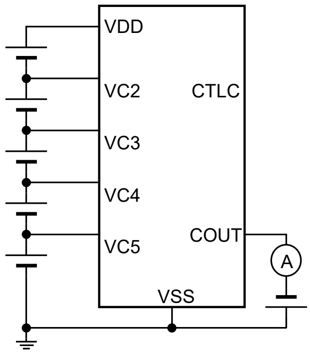

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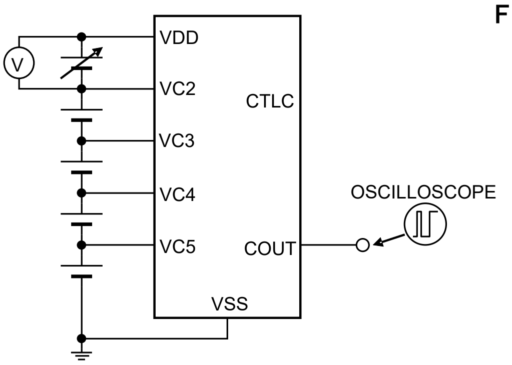

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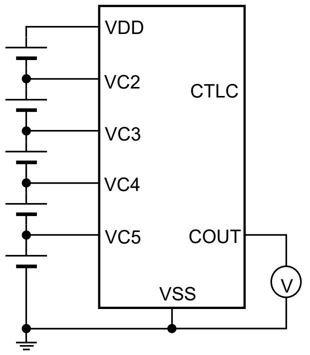

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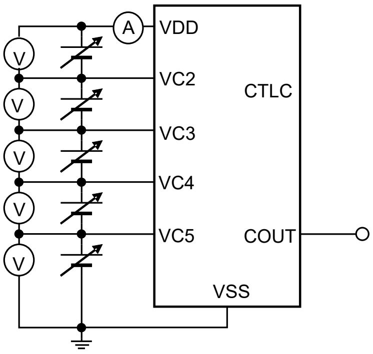

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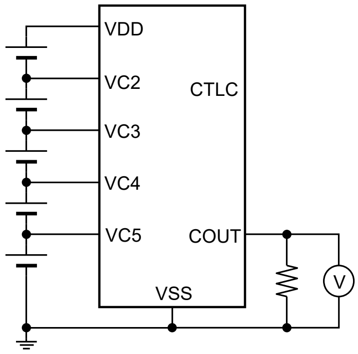

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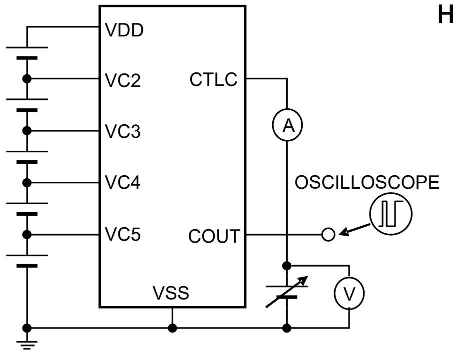

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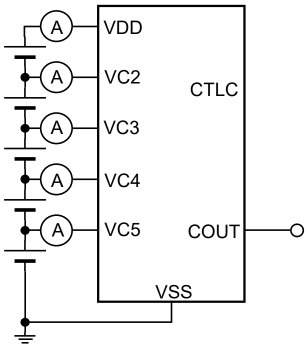


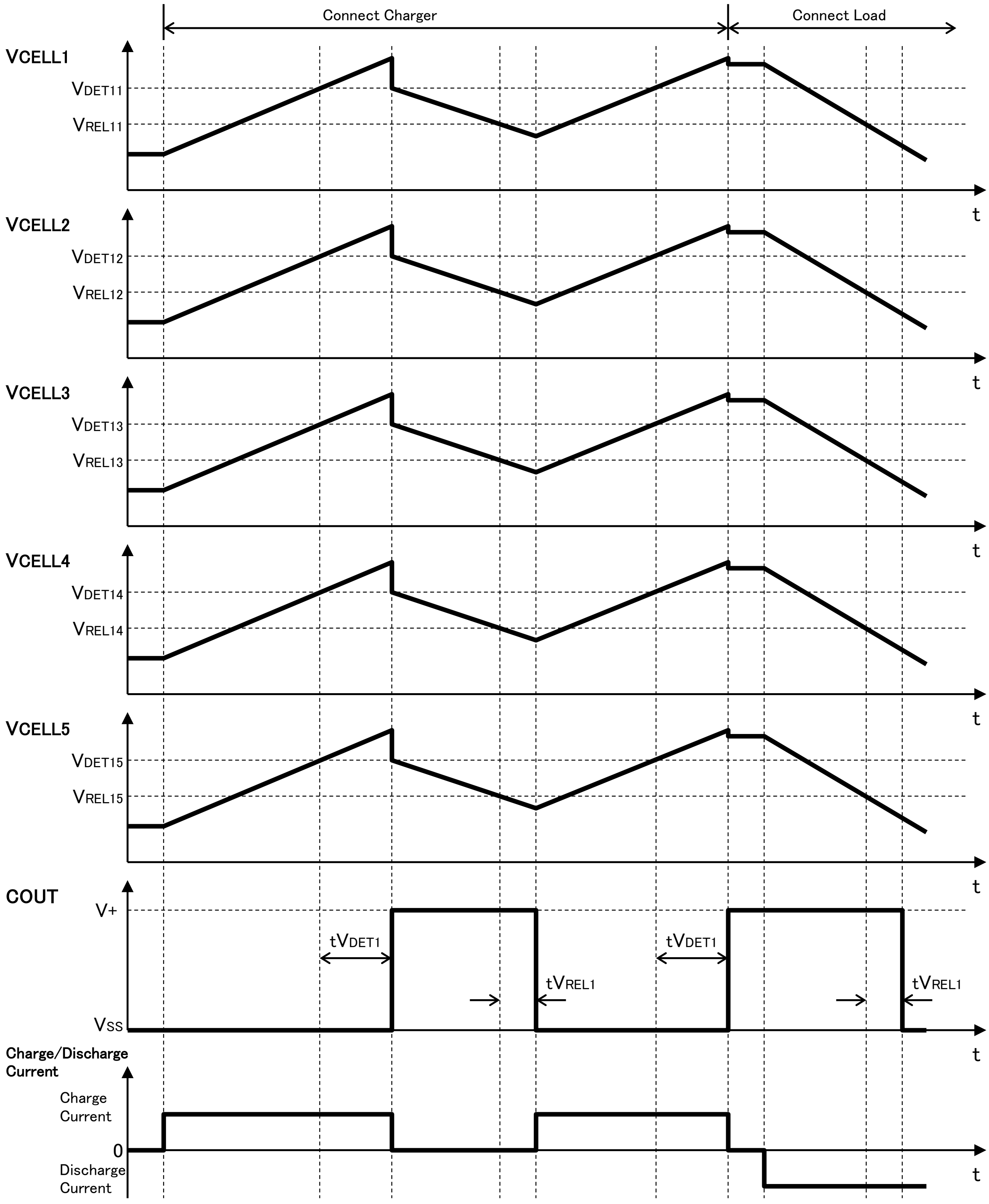
THEORY OF OPERATION

Overcharge Detector, V_{DET1n} (n = 1, 2, 3, 4, 5)

During charging, the device supervises the voltage between VDD pin and VC2 pin (V_{CELL1}), the voltage between VC2 pin and VC3 pin (V_{CELL2}), the voltage between VC3 pin and VC4 pin (V_{CELL3}), the voltage between VC4 pin and VC5 pin (V_{CELL4}), and the voltage between VC5 pin and VSS pin (V_{CELL5}). If at least one of the cell voltages exceeds more than the overcharge detection voltage (V_{DET1n}), the overcharge is detected, and an external charge control Nch. MOSFET turns on with COUT pin being at "H" level and by cutting a fuse on the charger path, and charge stops. If all the cell voltages become lower than the overcharge release voltage (V_{REL1n}), the overcharge is released and COUT pin outputs “Hiz”.

The device has internal fixed output delay times for overcharge detection, overcharge detection timer reset, and overcharge release. If the output delay time passes on when any one of the cell voltages is more than V_{DET1n}, the overcharge is detected. In the case of Timer Reset Delay available version, if all the cell voltages become lower than V_{DET1n} within the overcharge detection delay time by noise or other reasons, the time period is less than overcharge detection timer reset delay time, the overcharge delay time is accumulated and maintained, and the accumulated delay time reaches the overcharge detection delay time, the overcharge is detected. After detecting overcharge, even if all the cell voltages reduce less than the release voltage, if at least one of the cell voltages exceeds more than the release voltage within the overcharge release delay time, then overcharge is not released.

The COUT pin, which is a Pch. open-drain output type, outputs the output voltage of the internal regulator when “High”.



Overcharge Operation Timing Chart

Shutdown Function

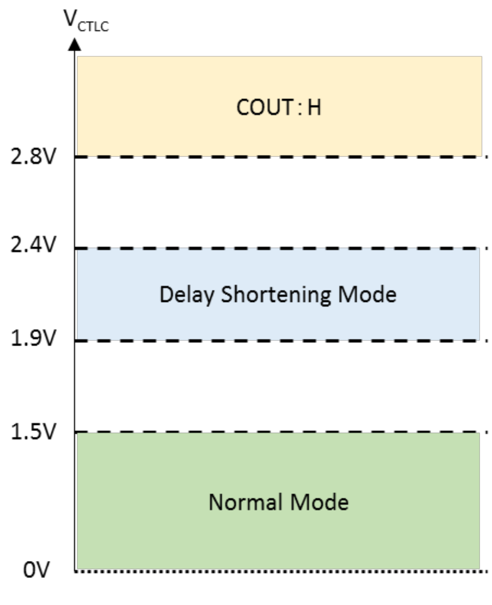
The voltage between VDD pin and VC2 pin (V_{CELL1}), the voltage between VC2 pin and VC3 pin (V_{CELL2}), the voltage between VC3 pin and VC4 pin (V_{CELL3}), the voltage between VC4 pin and VC5 pin (V_{CELL4}), and the voltage between VC5 pin and VSS pin (V_{CELL5}) are supervised. If all of V_{CELLn} (n=1 to 5) become less than the shutdown detection voltage, the device halts the operation, and the supply current (shutdown current) of the device can be reduced to the minimum. If one of V_{CELLn} (n=1 to 5) becomes more than the shutdown detection voltage, the device will release from the shutdown state.

CTLC Function

When exceeding the CTLC detection delay time or more after supplying the voltage of 2.8 V or more to CTLC pin, the COUT pin outputs “High” level. This function is enabled even in the shutdown state.
By cascading between the COUT pin of the high-voltage side IC and the CTLC pin of the low-voltage side IC, these devices can protect the battery pack for six or more series cell [1]. At cascading, the COUT pin output of the high-voltage side is transmitted to the CTLC pin of the low-voltage side and the COUT pin outputs “High”.

Delay Shortening (DS)

Applying the voltage of 1.9 V to 2.4 V to the CTLC pin can shorten the overcharge detection delay time to a few milliseconds (ms).



[1] Refer to *10-CELL PROTECTION CIRCUIT AT CASCADING in APPLICATION INFORMATION*.

Setting for 2 to 5 Cells Protection

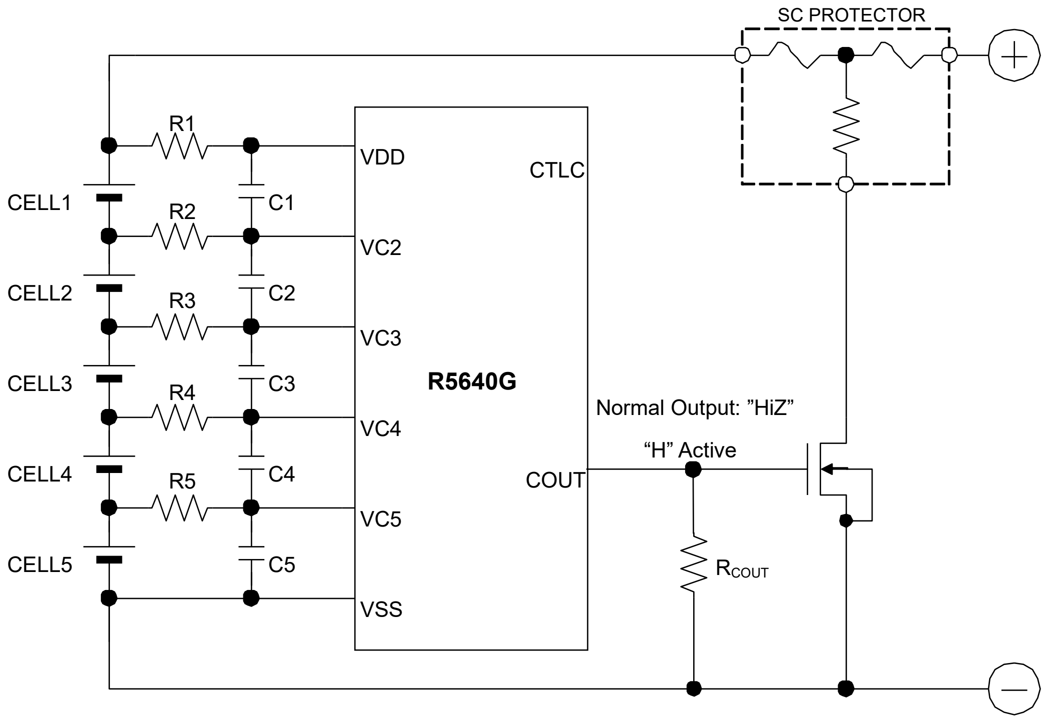
By short-circuiting between cells, the device can meet as a protection IC for 2 to 5 cells connected in series.

The following table indicates pins to short-circuit to VSS depending on protected cells.

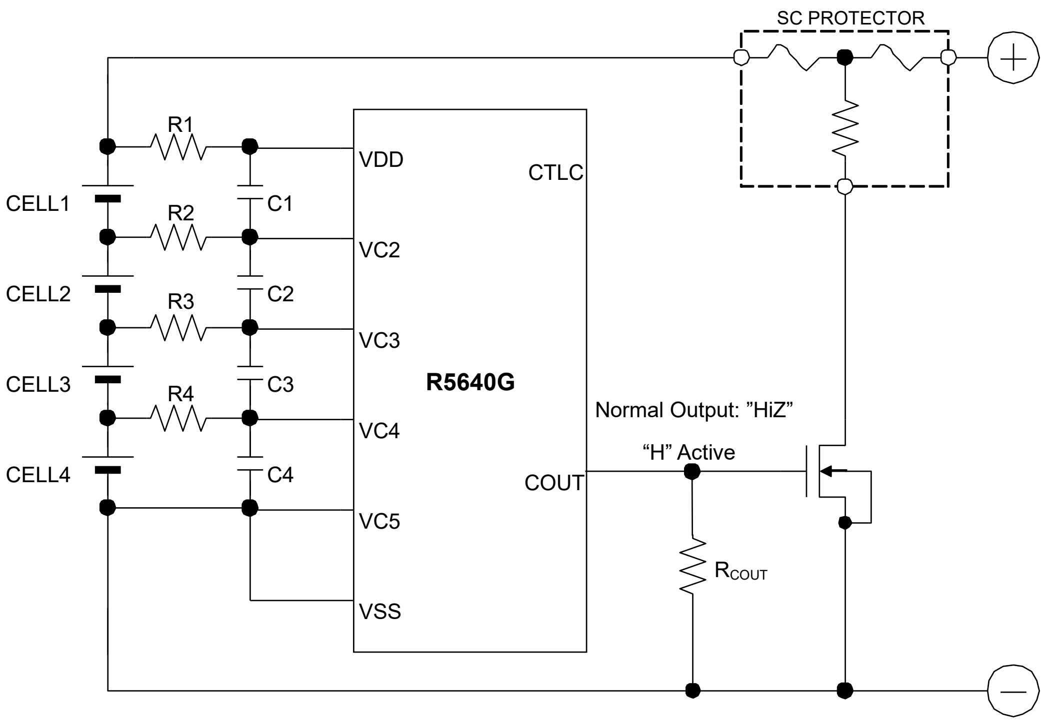
Protected Cells	Pins Short-circuiting to VSS
2-cell protection	VC3, VC4, and VC5 pins
3-cell protection	VC4 and VC5 pins
4-cell protection	VC5 pin
5-cell protection	Not short-circuiting

APPLICATION INFORMATION

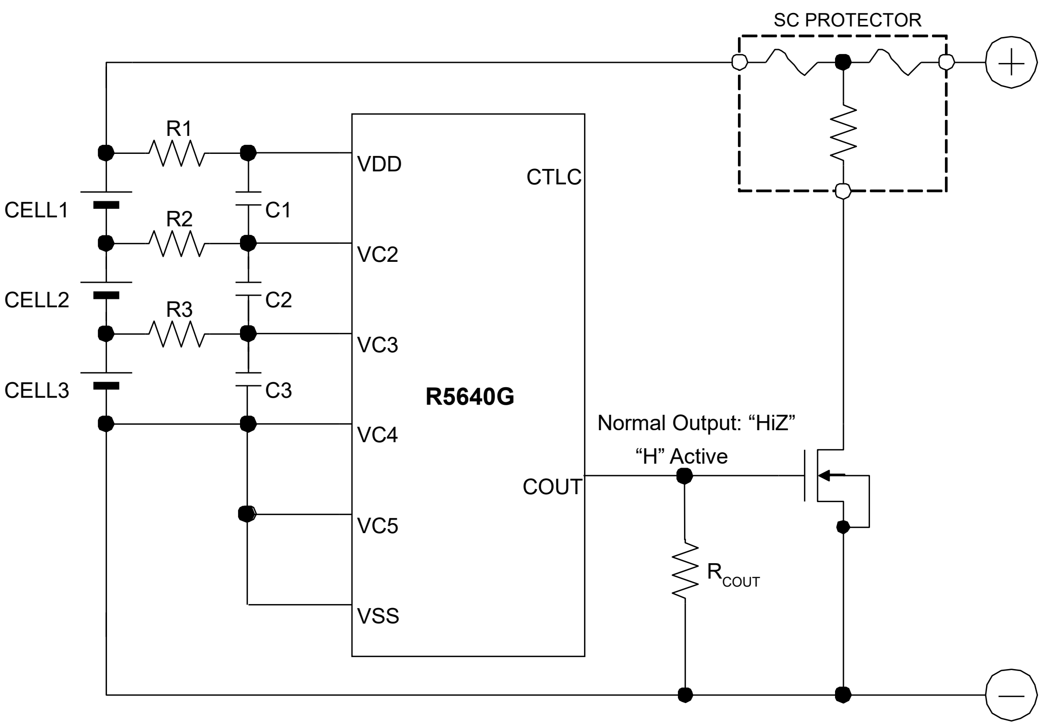
Typical Application Circuits



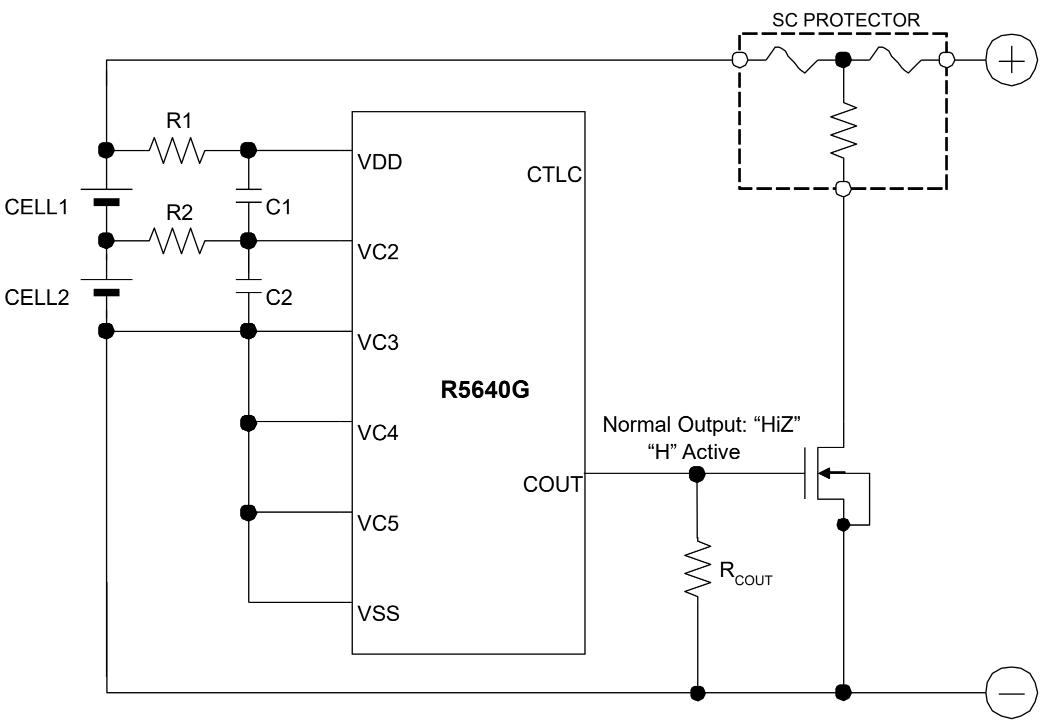
5-cell Protection Circuit



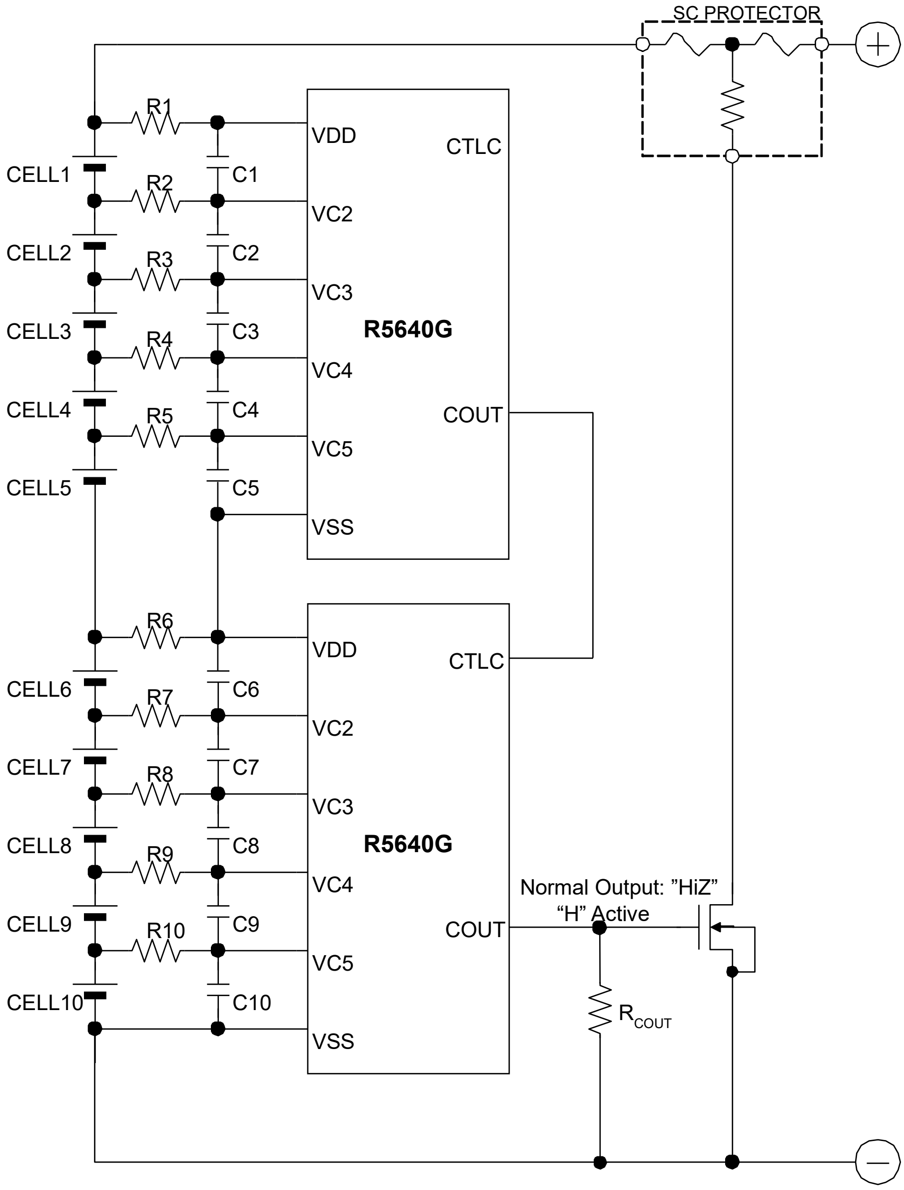
4-cell Protection Circuit



3-cell Protection Circuit



2-cell Protection Circuit



10-cell Protection Circuit at Cascading

External Components

Symbol	Typ.	Unit	Permissible Range
R1 / R2 / R3 / R4 / R5	330	Ω	330 to 1000
C1 / C2 / C3 / C4 / C5	0.1	μF	0.01 to 1
R_{COUT}	1	MΩ	0.5 to 2

Technical Notes on Component Selection

- The voltage fluctuation is stabilized with R1 to R5 and C1 to C5. Since increasing resistors of R1 to R5 make the detection voltage be higher by the conduction current at detection, the appropriate value of R1 to R5 must be less than 1kΩ. And the appropriate value of C1 to C5 must be 0.01μF or more in order to make a stable operation of the IC.

- If R_{COUT} is small, the supply current of the protect circuit will increase when the COUT pin is “high”.

- The typical application circuits are just examples and do not guarantee the operation. Conduct the sufficient evaluation in the actual application circuit in order to select external components.

- The protection IC and external components must not be applied overvoltage and overcurrent beyond the absolute maximum ratings. Especially, after detecting overcharge, a large heater current might flow through the MOSFET during the fuse blowout time. To prevent the MOSFET from being burnt, select a MOSFET with considering a current capacity of it.

- To connect the SC protector, connect the SC protector to the cell must be the last.

Contact Information for Inquiries regarding SC PROTECTOR

Dexerials Corporation (Sony Chemical & Information Device Company Ltd.)
URL: http://www.dexerials.jp

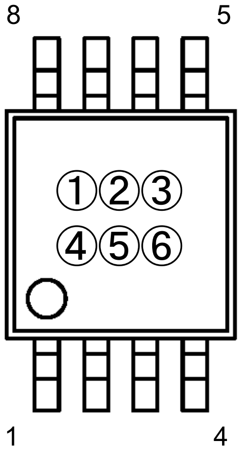
TECHNICAL NOTES

A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points.

- Please evaluate the product at the PCB level before use, as some symptoms may remain that cannot be confirmed by the evaluation at the IC level.
- When using any coating or underfill to improve moisture resistance or joining strength, evaluate them adequately before using. In certain materials or coating conditions, corrosion by contained constituents, current leakage by moisture absorption, crack and delamination by physical stress can happen. If the curing temperature of the coating material or underfill material exceeds the absolute maximum rating, the electrical characteristics of this product may change.
- When performing X-ray inspection in mass production process and evaluation build stage such as the product functions and characteristics confirmation, please confirm X-ray irradiation does not exceed 1.5Gy (absorbed dose for air).

①②③④: Product Code ··· Refer to *Part Marking List*

⑤⑥: Lot Number ··· Alphanumeric Serial Number



R5640G (MSOP-8) Part Markings

NOTICE
There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

R5640Gxxxxx Part Marking List

Product Name	①	②	③	④
R5640G301BA	R	0	1	A
R5640G302BA	R	0	2	A
R5640G305BB	R	0	3	A
R5640G251DA	R	0	4	A
R5640G252AB	R	0	5	A
R5640G101BB	R	0	7	A
R5640G254AB	R	0	8	A
R5640G471AA	R	0	9	A
R5640G472AA	R	1	0	A
R5640G256AB	R	1	1	A
R5640G302DA	R	1	2	A

Product Name	①	②	③	④
R5640G102AA	R	1	3	A
R5640G352BA	R	1	4	A

PD-MSOP-8(85125)-JE-B

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

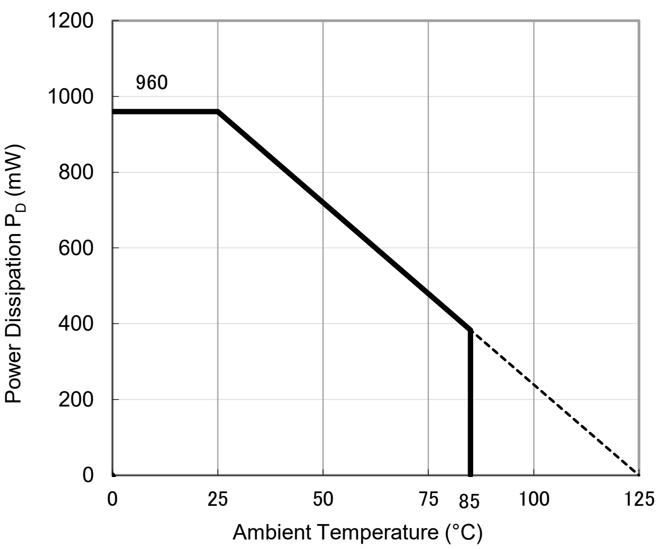
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 36 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

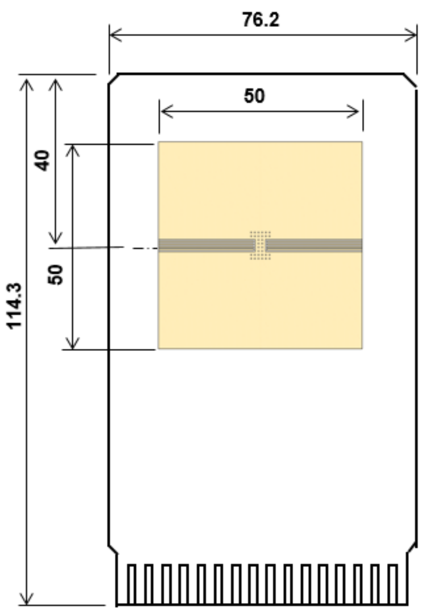
Item	Measurement Result
Power Dissipation	960 mW
Thermal Resistance (θja)	θja = 104°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 31°C/W

θja: Junction-to-Ambient Thermal Resistance

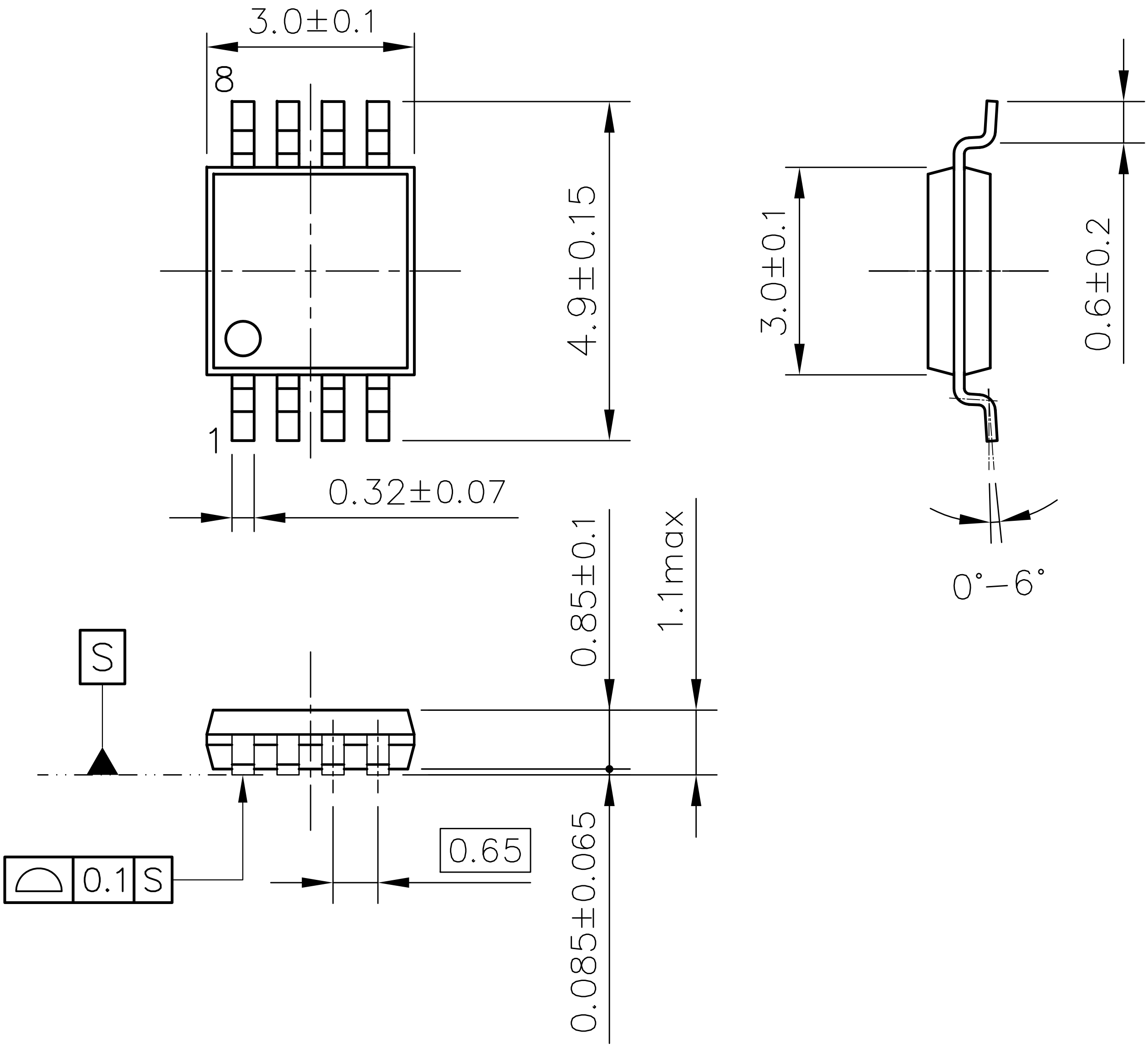
ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



MSOP-8 Package Dimensions (Unit: mm)

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Nisshinbo Micro Devices Inc.

Official website
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