RICOH

42 V Input 4ch Window Voltage Detector for Industrial Applications

No. EY-521-210302

OVERVIEW

The R3500S is a 4ch window voltage detector with manual reset function suited for systems requiring functional safety. This device monitors over and under voltage from the multiple power supplies to SoCs, memories and sensors to continuously supervise the system operating at normal voltage. This is a highreliability semiconductor device for industrial applications (-Y) that has passed both the screening at high temperature and the reliability test with extended hours.

KEY BENEFITS

- Power supply from battery enables the voltage detector to operate independently from the power source.
- High-accuracy detection of the over and under voltages from -1.25% to 0.75% and the hysteresis of Max. 0.75%.
- Management of multiple power supplies with a single chip to save space.

KEY SPECIFICATIONS

- Operating Voltage Range (Max. Rating):
 - 3.0 V to 42.0 V (50.0 V)
- Operating Temperature Range: -40°C to 125°C
- Supply Current: Typ. 10 µA
- Overvoltage Detection: 1.0 V to 5.9 V (0.01 V step)
- Undervoltage Detection: 0.9 V to 5.0 V (0.01 V step)
- Detection Release Hysteresis: Max. 0.75%

(-40°C to 125°C)

- Detection Voltage Accuracy:
 - $\pm 0.5\%$ (Ta = 25°C)
 - -1.25% to 0.75% (-40°C to 125°C)
- Detection Delay Time: Typ.20 µs
- Release Delay Time: Typ. 4 ms ($C_D = 0.01 \ \mu F$)
- Output Type: Nch. Open Drain

SELECTION GUIDE

Product Name	Package	Quantity per Reel
R3500SxxxA-E2-YE	HSOP-18	1,000 pcs

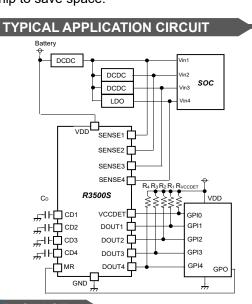
xxx: The combination of an overvoltage detection setting voltage (VOVSET) and an undervoltage detection setting voltage (V_{UVSET}) applied to 4ch.

Refer to "Product-Specific Electrical Characteristic" for details

APPLICATIONS

- Factory Automation Equipment, Smart meters
- High Temperature Devices: Surveillance Cameras and Vending Machines
- Self-heating Devices: Motors and Lightings





PACKAGE



5.2 x 6.2 x 1.45 (mm)

SELECTION GUIDE

The overvoltage detection setting voltage (V_{OVSET}) and the undervoltage detection setting voltage (V_{UVSET}) are user-selectable options.

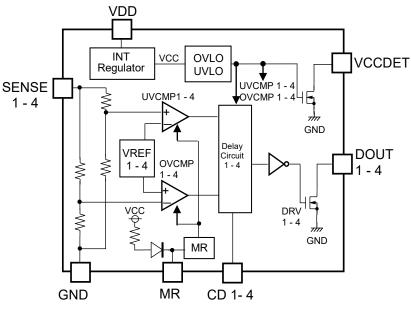
Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R3500SxxxA-E2-YE HSOP-1		1,000 pcs	Yes	Yes

xxx: The combination of an overvoltage detection setting voltage (V_{OVSET}) and an undervoltage detection setting voltage (V_{UVSET}).

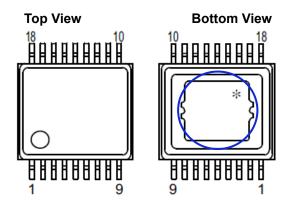
Refer to Product-specific Electrical Characteristics for more details.

BLOCK DIAGRAM



R3500S Block Diagram

PIN DESCRIPTIONS



R3500S (HSOP-18) Pin Configuration

* The tab on the bottom of the package shown by blue circle is substrate potential (GND). It is recommended that this tab be connected to the ground plane pin on the board.

R3500S Pin Description	escription	n D	Ρ)0S	R350
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Pin No.	Symbol	Description
1	VDD	Supply Voltage Pin
2	NC	No Connection ⁽¹⁾
3	VCCDET ⁽²⁾	Over/Under Voltage Detection for Internal Supply Output Pin ("Low" at detection)
4	SENSE1	VD Voltage SENSE Pin 1
5	SENSE2	VD Voltage SENSE Pin 2
6	SENSE3	VD Voltage SENSE Pin 3
7	SENSE4	VD Voltage SENSE Pin 4
8	NC	No Connection
9	MR	Manual Reset Pin ("Low" at reset)
10	GND	GND Pin
11	CD4	VD Release Delay Time Set Pin 4 ("OPEN" when not connected)
12	CD3	VD Release Delay Time Set Pin 3 ("OPEN" when not connected)
13	CD2	VD Release Delay Time Set Pin 2 ("OPEN" when not connected)
14	CD1	VD Release Delay Time Set Pin 1 ("OPEN" when not connected)
15	DOUT4 ⁽³⁾	Over/Under Voltage Detection Output Pin 4 ("Low" at detection)
16	DOUT3 ⁽³⁾	Over/Under Voltage Detection Output Pin 3 ("Low" at detection)
17	DOUT2 ⁽³⁾	Over/Under Voltage Detection Output Pin 2 ("Low" at detection)
18	DOUT1 ⁽³⁾	Over/Under Voltage Detection Output Pin 1 ("Low" at detection)

⁽¹⁾ NC pin should be set to "OPEN".

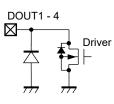
⁽²⁾ VCCDET pin is required to pull up to a suitable voltage with an external resistor.

⁽³⁾ DOUT1 to 4 pins are required to pull up to a suitable voltage with an external resistor.

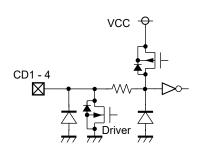
No. EY-521-210302

Internal Equivalent Circuit for Each Pin

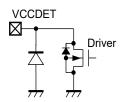
DOUT1 to 4 Pin

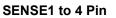


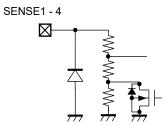
CD1 to 4 Pin



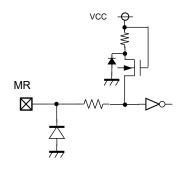












No. EY-521-210302

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
M	Supply Voltage	-0.3 to 50.0	V
V _{DD}	Peak Voltage ⁽¹⁾	60	V
VCD1 to 4	CD1 to 4 Pin Output Voltage	-0.3 to 20.0	V
VDOUT1 to 4	DOUT1 to 4 Pin Output Voltage	-0.3 to 20.0	V
VVCCDET	VCCDET Pin Output Voltage	-0.3 to 20.0	V
VSENSE1 to 4	SENSE1 to 4 Pin Input Voltage	-0.3 to 20.0	V
Vmr	MR Pin Voltage	-0.3 to 20.0	V
IDOUT1 to 4	DOUT1 to 4 Pin Output Current	30	mA
IVCCDET	VCCDET Pin Output Current	15	mA
PD	Power Dissipation	Refer to Appen <i>"POWER DISSIPA</i>	
Tj	Junction Temperature Range	-40 to 150	°C
Tstg	Storage Temperature Range	−55 to 150	°C

Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V _{DD}	Operating Voltage	3.0 to 42	V
VSENSE1 to 4	SENSE 1 to 4 Pin Input Voltage	0 to 6.0	V
V _{MR}	MR Pin Voltage	0 to 6.0	V
Та	Operating Temperature Range	-40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

⁽¹⁾ Duration Time: within 200 ms

ELECTRICAL CHARACTERISTICS

 V_{DD} = 14 V, C_D = 0.01 μ F, pulled-up to 5 V with 100 k Ω , unless otherwise specified.

The specifications surrounded by are guaranteed by design engineering at $-40^{\circ}C \le Ta \le 125^{\circ}C$.

R3500S (-YE) Electrical Characteristics(Ta= 25°C)						
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
	Overvoltage (OV)	Overvoltage (OV) $Ta = 25^{\circ}C$			x1.005	V
VOVDET1 to 4	Detector Threshold	–40°C ≤ Ta ≤ 125°C	x0.9875		x1.0075	V
	Undervoltage (UV)	Ta = 25°C	x0.995		x1.005	V
VUVDET1 to 4	Detector Threshold	–40°C ≤ Ta ≤ 125°C	x0.9875		x1.0075	V
VOVHYS1 to 4	Overvoltage (OV) Threshold Hysteresis		V _{OVDET} ×0.0025	V _{OVDET} ×0.005	V _{OVDET} ×0.0075	V
VUVHYS1 to 4	Undervoltage (UV) Threshold Hysteresis		V _{UVDET} ×0.0025	V _{UVDET} ×0.005	V _{UVDET} ×0.0075	V
I _{SS}	Supply Current	V _{DD} = 42 V, V _{UVDET} < V _{SENSE} < V _{OVDET}		10	25	μA
RSENSE1 to 4	SENSE1 to 4 Pin Resistance ⁽¹⁾		2.5		30	MΩ
Vuvlo	UVLO Detector Voltage			1.8	2.8	V
VUVLOHYS	UVLO Threshold Hysteresis			0.1	0.2	V
VDDLDOUT1 to 4	Supply Voltage with Low-operating DOUT1 to 4 Pin Output Voltage ⁽²⁾				1.7	V
DOUT1 to 4	DOUT1 to 4 Pin Driver Output Current	V _{DD} = 3.0, V _{DS} = 0.1 V	0.37	0.75	1.5	mA
LEAK1 to 4	DOUT1 to 4 Pin Leak Current	V _{DOUT1 to 4} = 5.5 V		0	1.0	μA
V _{MRH}	MR Input Voltage "High"		1.6			V
V _{MRL}	MR Input Voltage "Low"				0.5	V
t DELAY1 to 4	Release Delay Time	C _D = 0.01 µF	2.5	4	8	ms
IVCCDET	VCCDET Pin Driver Output Current	V _{DD} = 3.0, V _{DS} = 0.1 V	0.15	0.4	0.8	mA
ILEAKVCCDET	VCCDET Pin Driver Leakage Current	V _{DS} = 5.5 V		0	0.3	μA

All test items listed in Electrical Characteristics are done under the pulse load condition (Tj \approx Ta = 25°C).

⁽¹⁾ Typ. value is varied depending on the set value of detection voltage.

⁽²⁾ Minimum value of the power supply voltage when the detection output voltage becomes 0.1 V or lower.

(Pull-up resistance: 100 k Ω , Pull-up voltage: 5 V)

 V_{DD} = 14 V, C_{D} = 0.01 $\mu F,$ pulled-up to 5 V with 100 k $\Omega,$ unless otherwise specfied.

			VUVDET (V)			VOVDET (V)	
Product nar	ne	Min.	Тур.	Max.	Min.	Max.	
	1ch	4.796	4.82	4.844	5.184	Typ. 5.21	5.236
	2ch	3.165	3.18	3.195	3.413	3.43	3.447
R3500S001A	3ch	1.732	1.74	1.748	1.861	1.87	1.879
	4ch	1.055	1.06	1.065	1.135	1.14	1.145
	1ch	4.796	4.82	4.844	5.184	5.21	5.236
R3500S002A	2ch	3.165	3.18	3.195	3.413	3.43	3.447
	3ch	1.732	1.74	1.748	1.861	1.87	1.879
	4ch	1.155	1.16	1.165	1.244	1.25	1.256
	1ch	4.796	4.82	4.844	5.184	5.21	5.236
	2ch	3.165	3.18	3.195	3.413	3.43	3.447
R3500S003A	3ch	1.443	1.45	1.457	1.553	1.56	1.567
	4ch	0.966	0.97	0.974	1.035	1.04	1.045
	1ch	4.796	4.82	4.844	5.184	5.21	5.236
	2ch	3.165	3.18	3.195	3.413	3.43	3.447
R3500S004A	3ch	2.398	2.41	2.422	2.587	2.60	2.613
	4ch	1.055	1.06	1.065	1.135	1.14	1.145
	1ch	0.966	0.97	0.974	1.025	1.03	1.035
	2ch	1.702	1.71	1.718	1.881	1.89	1.899
R3500S005A	3ch	1.702	1.71	1.718	1.881	1.89	1.899
	4ch	3.125	3.14	3.155	3.453	3.47	3.487
	1ch	0.946	0.95	0.954	1.045	1.05	1.055
	2ch	1.155	1.16	1.165	1.244	1.25	1.256
R3500S006A	3ch	1.702	1.71	1.718	1.881	1.89	1.899
	4ch	3.125	3.14	3.155	3.453	3.47	3.487
	1ch	0.946	0.95	0.954	1.045	1.05	1.055
D05000074	2ch	1.274	1.28	1.286	1.413	1.42	1.427
R3500S007A	3ch	1.702	1.71	1.718	1.881	1.89	1.899
	4ch	3.125	3.14	3.155	3.453	3.47	3.487
	1ch	1.125	1.13	1.135	1.364	1.37	1.376
D25000000	2ch	2.985	3.00	3.015	3.582	3.60	3.618
R3500S008A	3ch	3.125	3.14	3.155	3.453	3.47	3.487
	4ch	3.125	3.14	3.155	3.453	3.47	3.487
	1ch	3.025	3.04	3.055	3.553	3.57	3.587
R3500S009A	2ch	3.025	3.04	3.055	3.553	3.57	3.587
N33003009A	3ch	0.916	0.92	0.924	1.085	1.09	1.095
	4ch	0.916	0.92	0.924	1.085	1.09	1.095
	1ch	4.538	4.56	4.582	5.423	5.45	5.477
R3500S010A	2ch	2.995	3.01	3.025	3.582	3.60	3.618
K35003010A	3ch	1.135	1.14	1.145	1.354	1.36	1.366
	4ch	1.165	1.17	1.175	1.403	1.41	1.417
	1ch	2.727	2.74	2.753	3.264	3.28	3.296
R3500S011A	2ch	1.632	1.64	1.648	1.961	1.97	1.979
NJJUUJUTIA	3ch	0.966	0.97	0.974	1.234	1.24	1.246
	4ch	2.995	3.01	3.025	3.582	3.60	3.618

R3500S (-YE) Product-specific Electrical Characteristics

(Ta = 25°C)

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 $V_{DD} = 14 \text{ V}, C_D = 0.01 \mu\text{F}, \text{ pulled-up to 5 V with 100 k}\Omega, \text{ unless otherwise specified.}$ The specifications surrounded by ______ are guaranteed by design engineering at $-40^{\circ}\text{C} \le \text{Ta} \le 125^{\circ}\text{C}.$

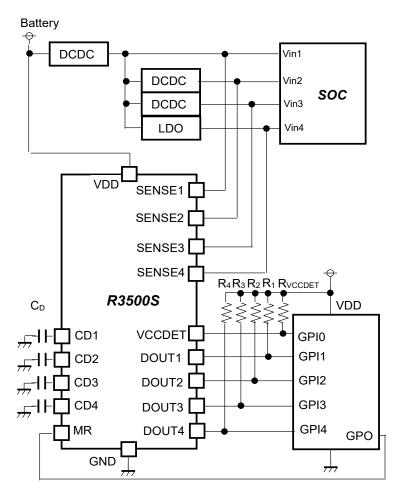
R3500S (-Y	E) Product-sp	ecific Electrical	Characteristics
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(–40°C ≤ Ta ≤ 125°C)

	-	VUVDET (V)		1	VOVDET (V)		VUVHYS (V)		<u>(-40 0 1 12 120 0)</u> Vovнys (V)				
Product na	ame	Min.	Typ.	, Max.	Min.	Typ.	/ Max.	Min.	Typ.	, Max.	Min.	Typ.	/ Max.
	1ch	4.760	4.82	4.856	5.145	5.21	5.249	0.013	0.024	0.036	0.014	0.026	0.039
	2ch	3.141	3.18	3.203	3.388	3.43	3.455	0.008	0.016	0.023	0.009	0.017	0.025
R3500S001A	3ch	1.719	1.74	1.753	1.847	1.87	1.884	0.005	0.009	0.013	0.005	0.009	0.014
	4ch	1.047	1.06	1.067	1.126	1.14	1.148	0.003	0.005	0.007	0.003	0.006	0.008
	1ch	4.760	4.82	4.856	5.145	5.21	5.249	0.013	0.024	0.036	0.014	0.026	0.039
	2ch	3.141	3.18	3.203	3.388	3.43	3.455	0.008	0.016	0.023	0.009	0.017	0.025
R3500S002A	3ch	1.719	1.74	1.753	1.847	1.87	1.884	0.005	0.009	0.013	0.005	0.009	0.014
	4ch	1.146	1.16	1.168	1.235	1.25	1.259	0.003	0.006	0.008	0.004	0.006	0.009
	1ch	4.760	4.82	4.856	5.145	5.21	5.249	0.013	0.024	0.036	0.014	0.026	0.039
	2ch	3.141	3.18	3.203	3.388	3.43	3.455	0.008	0.016	0.023	0.009	0.017	0.025
R3500S003A	3ch	1.432	1.45	1.460	1.541	1.56	1.571	0.004	0.007	0.010	0.004	0.008	0.011
	4ch	0.958	0.97	0.977	1.027	1.04	1.047	0.003	0.005	0.007	0.003	0.005	0.007
		4.760	4.82	4.856	5.145	5.21	5.249	0.013	0.024	0.036	0.014	0.026	0.039
	1ch	3.141	3.18	3.203	3.388	3.43	3.455	0.008	0.016	0.023	0.009	0.017	0.025
R3500S004A	2ch	2.380	2.41	2.428	2.568	2.60	2.619	0.007	0.012	0.018	0.007	0.013	0.019
	3ch	1.047	1.06	1.067	1.126	1.14	1.148	0.003	0.005	0.007	0.003	0.006	0.008
	4ch	0.958	0.97	0.977	1.018	1.03	1.037	0.003	0.005	0.007	0.003	0.005	0.007
	1ch	1.689	1.71	1.722	1.867	1.89	1.904	0.005	0.009	0.007	0.005	0.009	0.007
R3500S005A	2ch	1.689	1.71	1.722	1.867	1.89	1.904	0.005	0.009	0.012	0.005	0.009	0.014
	3ch	3.101	3.14	3.163	3.427	3.47	3.496	0.005	0.009	0.012	0.005	0.009	0.014
	4ch												
	1ch	0.939	0.95	0.957	1.037	1.05	1.057	0.003	0.005	0.007	0.003	0.005	0.007
R3500S006A	2ch	1.146	1.16	1.168	1.235	1.25	1.259	0.003	0.006	0.008	0.004	0.006	0.009
	3ch	1.689	1.71	1.722	1.867	1.89	1.904	0.005	0.009	0.012	0.005	0.009	0.014
	4ch	3.101	3.14	3.163	3.427	3.47	3.496	0.008	0.016	0.023	0.009	0.017	0.026
	1ch	0.939	0.95	0.957	1.037	1.05	1.057	0.003	0.005	0.007	0.003	0.005	0.007
R3500S007A	2ch	1.264	1.28	1.289	1.403	1.42	1.430	0.004	0.006	0.009	0.004	0.007	0.010
	3ch	1.689	1.71	1.722	1.867	1.89	1.904	0.005	0.009	0.012	0.005	0.009	0.014
	4ch	3.101	3.14	3.163	3.427	3.47	3.496	0.008	0.016	0.023	0.009	0.017	0.026
	1ch	1.116	1.13	1.138	1.353	1.37	1.380	0.003	0.006	0.008	0.004	0.007	0.010
R3500S008A	2ch	2.963	3.00	3.022	3.555	3.60	3.627	0.008	0.015	0.022	0.009	0.018	0.027
	3ch	3.101	3.14	3.163	3.427	3.47	3.496	0.008	0.016	0.023	0.009	0.017	0.026
	4ch	3.101	3.14	3.163	3.427	3.47	3.496	0.008	0.016	0.023	0.009	0.017	0.026
	1ch	3.002	3.04	3.062	3.526	3.57	3.596	0.008	0.015	0.022	0.009	0.018	0.026
R3500S009A	2ch	3.002	3.04	3.062	3.526	3.57	3.596	0.008	0.015	0.022	0.009	0.018	0.026
	3ch	0.909	0.92	0.926	1.077	1.09	1.098	0.003	0.005	0.006	0.003	0.005	0.008
	4ch	0.909	0.92	0.926	1.077	1.09	1.098	0.003	0.005	0.006	0.003	0.005	0.008
	1ch	4.503	4.56	4.594	5.382	5.45	5.490	0.012	0.023	0.034	0.014	0.027	0.040
R3500S010A	2ch	2.973	3.01	3.032	3.555	3.60	3.627	0.008	0.015	0.022	0.009	0.018	0.027
	3ch	1.126	1.14	1.148	1.343	1.36	1.370	0.003	0.006	0.008	0.004	0.007	0.010
	4ch	1.156	1.17	1.178	1.393	1.41	1.420	0.003	0.006	0.008	0.004	0.007	0.010
	1ch	2.706	2.74	2.760	3.239	3.28	3.304	0.007	0.014	0.020	0.009	0.016	0.024
R3500S011A	2ch	1.620	1.64	1.652	1.946	1.97	1.984	0.005	0.008	0.012	0.005	0.010	0.014
1000000117	3ch	0.958	0.97	0.977	1.225	1.24	1.249	0.003	0.005	0.007	0.004	0.006	0.009
	4ch	2.973	3.01	3.032	3.555	3.60	3.627	0.008	0.015	0.022	0.009	0.018	0.027

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TYPICAL APPLICATION CIRCUIT



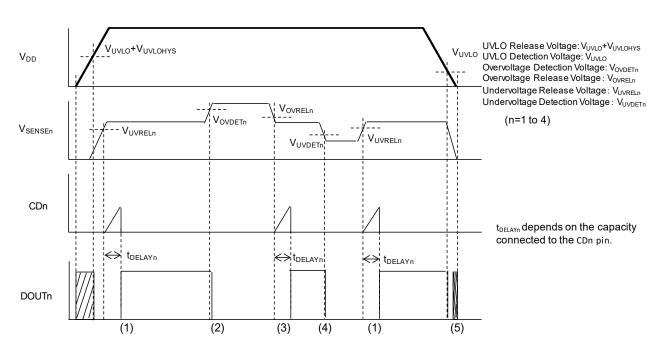
R3500S Typical Application

External Components

Symbol	Description
CD	Capacitors should be selected corresponding to the set Release Delay Time. Refer to <i>"Delay in Operation and Release Delay Time (t_{DELAY})"</i> in THEORY OF OPERATION for details. When the Release Delay Time is unnecessary, layout the circuit without any capacitors.
Rn Rvccdet	The on-resistance of the driver is max. 270 Ω calculated from the DOUTn (n=1 to 4) pin driver output current shown in <i>"Electrical Characteristics"</i> . The maximum voltage at DOUTn="Low" is determined by the maximum on-resistance, pull-up voltage and Rn. The off-resistance of the driver is min. 5.5 M Ω calculated from the driver leakage current shown in <i>"Electrical Characteristics"</i> . The minimum voltage at DOUTn="High" is determined by the minimum off-resistance, pull-up voltage and Rn. Set the VCCDET pin in the same way. <i>"Electrical Characteristic"</i> is evaluated in conditions that Pull-up voltage = 5 V and Rn = 100 k Ω . SENSEn and DOUTn pins should be set to open when they are not connected.

No. EY-521-210302

THEORY OF OPERATION



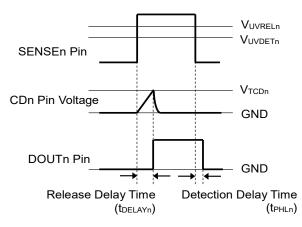
R3500S Timing Chart

- (1) When the SENSEn pin voltage (V_{SENSEn}) exceeds the undervoltage release voltage (V_{UVRELn}), the DOUTn pin outputs "High" after the release delay time (t_{DELAYn}).
- (2) When V_{SENSEn} exceeds the overvoltage detection voltage (V_{OVDETn}), the DOUTn pin outputs "Low" after the detection delay time (Typ.20 μs) and this triggers the overvoltage detecting state.
- (3) When V_{SENSEn} drops below the overvoltage release voltage (V_{OVRELn}), the DOUTn pin outputs "High" after the release delay time (t_{DELAYn}).
- (4) When V_{SENSEn} drops further below the undervoltage detection voltage (V_{UVDETn}), the DOUTn pin outputs "Low" after the detection delay time (Typ.20 μs) and this triggers the undervoltage detecting state.
- (5) When the VDD pin voltage (V_{DD}) drops below the UVLO detection voltage (V_{UVLO}), the DOUTn pin outputs "Low". Note that DOUTn cannot maintain "Low" when the VDD pin voltage drops further and becomes lower than V_{DDLDOUTn}.

Delay Operation and Release Delay Time (t_{DELAY})

At Undervoltage Detection

A higher voltage than the undervoltage release voltage (V_{UVRELn}) supplied to the SENSEn pin triggers charging of the external capacitor then the CDn pin voltage (V_{CDn}) increases. The DOUTn pin voltage (V_{DOUTn}) maintains "Low" until V_{CDn} reaches the CDn pin threshold voltage (V_{TCDn}). When V_{CDn} exceeds V_{TCDn} , V_{DOUTn} transitions from "Low" to "High". The release delay time (t_{DELAYn}) is the period until V_{DOUTn} transitions to "High" after the SENSEn pin voltage (V_{SENSEn}) exceeds V_{UVRELn} . The output voltage transitions from "Low" to "High" and it leads to discharging of the external capacitor. Without CD capacitors, the release delay time (Typ. 20 µs) becomes short depending on the circuit delay and CDn pin stray capacitance. When the lower voltage than V_{UVDETn} is supplied to the SENSEn pin, the detection delay time (t_{PHLn}) for which V_{DOUTn} transitions from "High" to "Low" is independent from the external capacitor and will be constant.



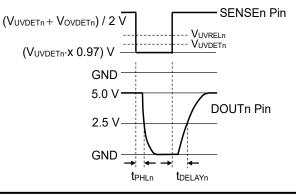
Undervoltage Release Delay Timing Diagram

Calculation of Release Delay Time (t_{DELAY})

The typical value of the release delay time (t_{DELAYn}) with the capacitance of the external capacitor (C_D) is calculated in the following equation:

 $t_{\text{DELAYn}}(s) = 0.73 \times C_{\text{D}}(\text{F}) / (1.8 \times 10^{-6})$

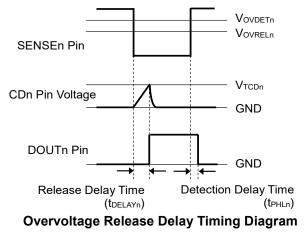
 t_{DELAYn} is the period until the DOUTn pin voltage (V_{DOUTn}) reaches 2.5 V after the pulse voltage of (V_{UVDETn}+V_{OVDETn}) /2 V increased from (V_{UVDETn} x 0.97) V is supplied to the SENSEn pin when V_{DOUTn} is pulled up to 5 V with 100 k Ω .



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At Overvoltage Detection

A lower voltage than the overvoltage release voltage (V_{OVRELn}) supplied to the SENSEn pin triggers charging of the external capacitor then the CDn pin voltage (V_{CDn}) increases. The DOUTn pin voltage (V_{DOUTn}) maintains "Low" until V_{CDn} reaches the CDn pin threshold voltage (V_{TCDn}). When V_{CDn} exceeds V_{TCDn} , V_{DOUTn} transitions from "Low" to "High". The release delay time (t_{DELAYn}) is the period until V_{DOUTn} transitions to "High" after the SENSEn pin voltage (V_{SENSEn}) exceeds V_{OVRELn} . The output voltage transitions from "Low" to "High" and it leads to discharging of the external capacitor. Without CD capacitors, the release delay time (Typ. 20 µs) becomes short depending on the circuit delay and CDn pin stray capacitance. When the higher voltage than V_{OVDETn} is supplied to the SENSEn pin, the detection delay time (t_{PHLn}) for which V_{DOUTn} transitions from "High" to "Low" is independent from the external capacitor and will be constant.

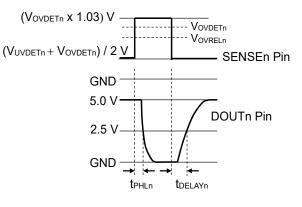


Calculation of Release Delay Time (t_{DELAY})

The typical value of the release delay time (t_{DELAYn}) with the capacitance of the external capacitor (C_D) is calculated in the following equation:

 $t_{\text{DELAYn}}(s) = 0.73 \times C_{\text{D}}(\text{F}) / (1.8 \times 10^{-6})$

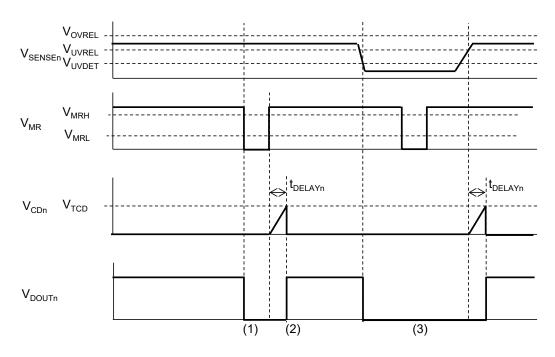
 t_{DELAYn} is the period until the DOUTn pin voltage (V_{DOUTn}) reaches 2.5 V after the pulse voltage of (V_{UVDETn}+V_{OVDETn}) /2 V decreased from (V_{OVDETn} x 1.03) V is supplied to the SENSEn pin when V_{DOUTn} is pulled up to 5 V with 100 k Ω .



RICOH

Manual Reset Function with MR Pin

The manual reset function is to set DOUTn to "Low" by inputting "Low" to the MR pin even when V_{SENSEn} is within a range of the release voltage. In other cases, set the MR pin voltage to "High" or open. In a system without using the manual reset function, set the MR pin voltage to "High" or open. (Pull-up resistance: Typ. 100 k Ω)



Manual Reset Timing Chart

- (1) When inputting "Low" to the MR pin, DOUTn is fixed to "Low" after the manual reset detection delay time (Typ. 20 μs) even if the SENSEn pin voltage (V_{SENSEn}) is within a range of the release voltage. The "Low" signal should be 50 μs or more.
- (2) When the MR pin transitions from "Low" to "High", DOUTn becomes "High" after the release delay time (t_{DELAYn}). At this time, the MR pin should maintain "High" for the release delay time or longer. Even if the external capacitor (CDn capacitance) is not connected, it should maintain "High" for 50 µs or more.
- (3) When V_{SENSEn} is lower than V_{UVDETn} or higher than V_{OVDETn}, and DOUTn is "Low", DOUTn does not transition even when the MR pin is set to "Low".

APPLICATION INFORMATION

Internal Supply Voltage Monitoring with VCCDET

The R3500 has a voltage regulator (INT regulator) inside the IC. Major functions of the IC are operated by VCC (Typ. 3.3V) generated by INT regulator from input voltage, VDD. The overvoltage detection circuit, OVLO and the undervoltage detection circuit, UVLO monitor the VCC being within the normal voltage range. When VCC is out of the normal range, NMOS driver connected to VCCDET pin turns on. By pulling up VCCDET pin, when OVLO or UVLO detects an abnormal VCC voltage, the output of VCCDET pin becomes "L". By monitoring VCC, UVLO also monitors undervoltage of VDD indirectly.

Even if pulled up VCCDET pin becomes "L", the R3500 doesn't lose the voltage detector function immediately. VCCDET pin should be set to open when it is unused.

R3500 Fault Detection Utilizing the Manual Reset Function

When a DOUTn pin output is "H", it's very important to know whether it's a result of normal voltage detector function or malfunction.

Utilizing the R3500 manual reset function, one part of IC faults can be detected. By the manual reset function, when "L" signal is input to MR pin, DOUTn pin output is fixed to "L" forcibly. If DOUTn pin doesn't become "L" even though SENSE pin voltage is within the released voltage range and "L" is input to MR pin, this can be determined as an IC fault.

When DOUTn is fixed to "H" due to an IC fault, DOUTn pin doesn't become "L" even "L" signal is input to MR pin. The faults can be detected with the manual reset function of the R3500 by checking DOUTn pin condition as above, are a wire open fault of DOUTn pin or an open fault of the output driver.

When detect IC faults with the manual reset function, follow the "Manual Reset Function with MR Pin" noted previously.

The system which usually receives output from DOUTn pin should not receive output from DOUTn pin during a fault detection test.

The concept of "H" level of MR pin

The R3500 has a voltage regulator (INT regulator) inside the IC. Major functions of the IC are operated by VCC (Typ. 3.3V) generated by INT regulator from input voltage, VDD.

MR pin is pulled up to VCC voltage via $100k\Omega$ as it can be set to open when MR pin is unused.

When the manual reset function is in use, when input "L" signal to MR pin, then DOUTn pin becomes "L". But when the manual reset function is in no use, if "H" voltage is input to MR pin, the current which is determined by the following equation flows continuously. This makes the supply current increase.

(VCC – MR "H" voltage) /100kΩ (VCC > MR "H" voltage)

Unless there's a specific reason to avoid an OPEN pin condition, it's recommended to be left OPEN when MR pin is not used.

As the circuit configuration prevents a reverse current from MR pin to VCC, even when being used in condition of MR "H" voltage>VCC, supply current doesn't increase and VCC voltage doesn't vary.

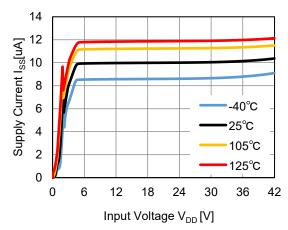
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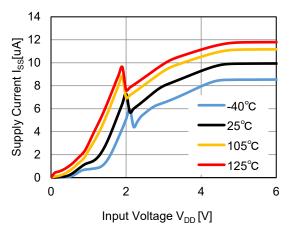
TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Supply Current vs. Input Voltage

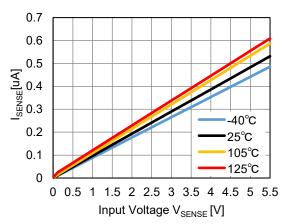
VUVSET = 4.82V / VOVSET = 5.21V, VUVSET = 3.18V / VOVSET = 3.43V, VUVSET = 1.74V / VOVSET = 1.87V, VUVSET = 0.97V / VOVSET = 1.04V



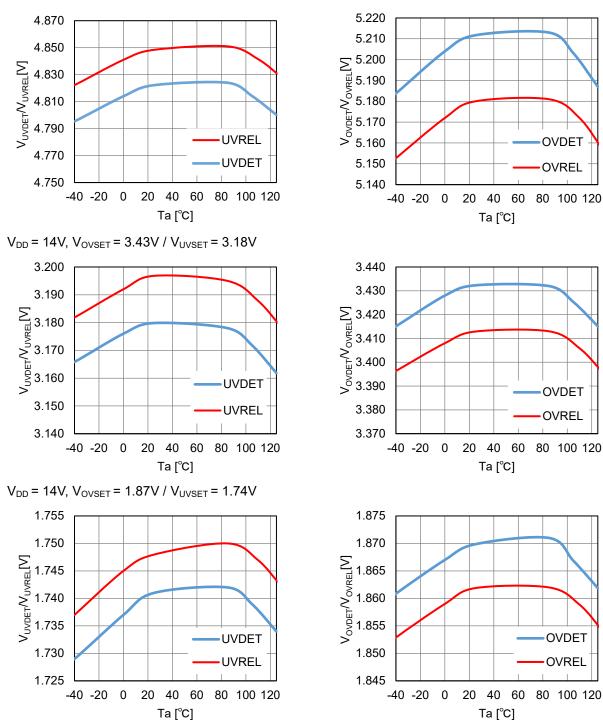


2) SENSE Current vs. Input Voltage

 $V_{UVSET} = 3.18V / V_{OVSET} = 3.43V$



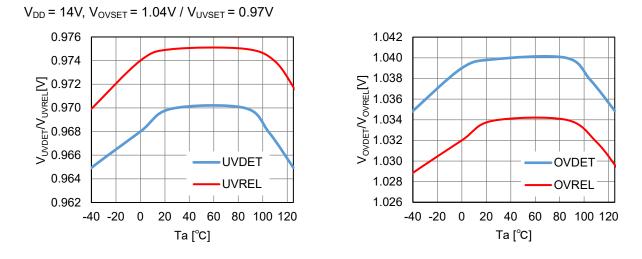
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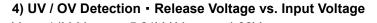


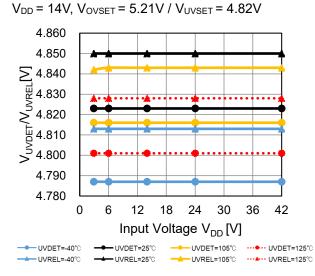
3) UV / OV Detection · Release Voltage vs. Temperature

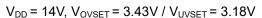
 V_{DD} = 14V, V_{OVSET} = 5.21V / V_{UVSET} = 4.82V

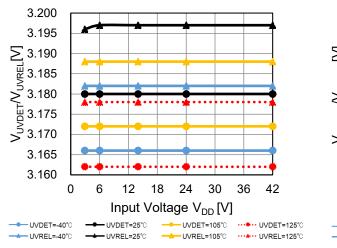
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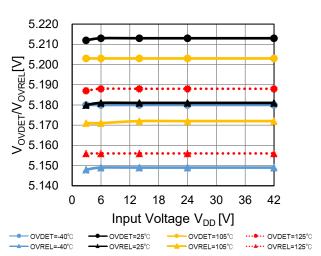


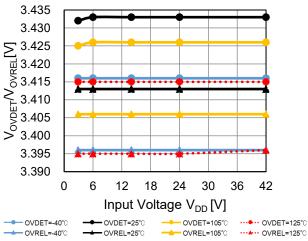






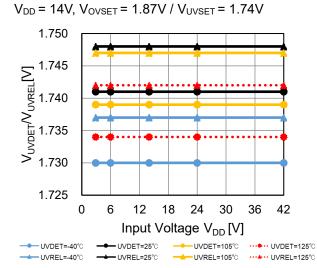


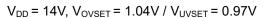


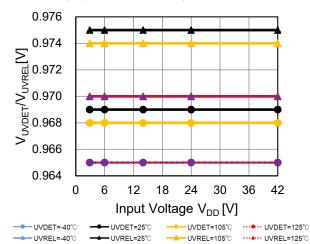


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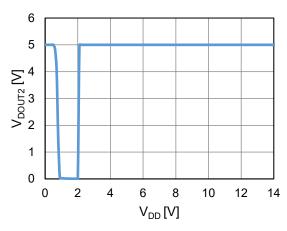
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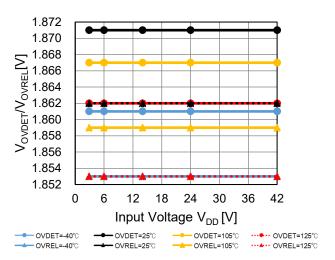


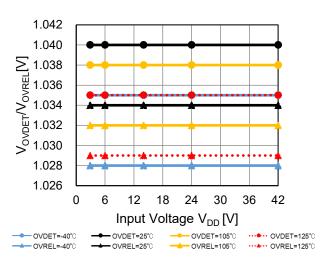




5) DOUT Pin Voltage vs. Input Voltage V_{SENSE} = (V_{OVSET}+V_{UVSET})/2, Pull-up Voltage = 5V



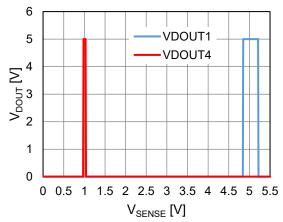




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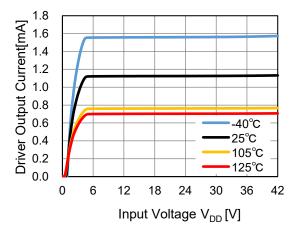
6) DOUT Pin Voltage vs. SENSE Pin Voltage

 $V_{\text{UVSET}} = 4.82 \text{V} / V_{\text{OVSET}} = 5.21 \text{V},$ $V_{\text{UVSET}} = 0.97 \text{V} / V_{\text{OVSET}} = 1.04 \text{V}, \text{ Pull-up Voltage} = 5 \text{V}$

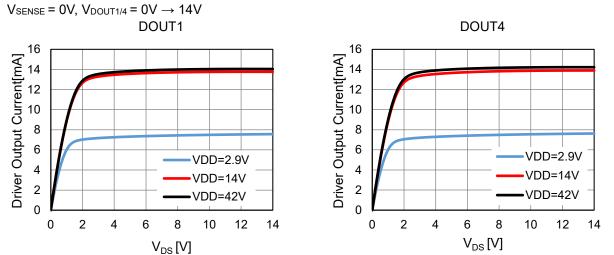


7) Driver Output Current vs. Input Voltage

VSENSE = 0V, VDOUT2 = 0.1V





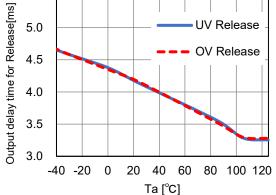


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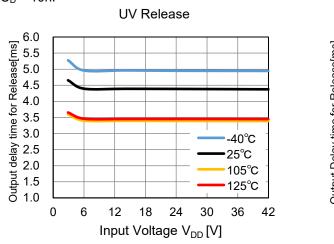
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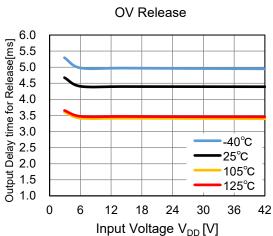
9) Release Delay Time vs. Temperature

 $V_{SENSE} = 0V \rightarrow (V_{UVSET} + V_{OVSET})/2 (UV)$ $V_{SENSE} = 5.5V \rightarrow (V_{UVSET} + V_{OVSET})/2 (OV), C_D = 10nF$ $\frac{5.5}{\frac{0}{2}} 5.0$ UV Release -

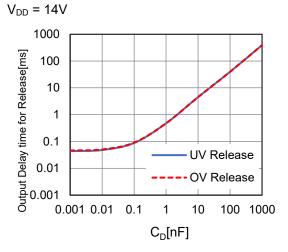


10) Release Delay Time vs. Input Voltage $C_D = 10nF$

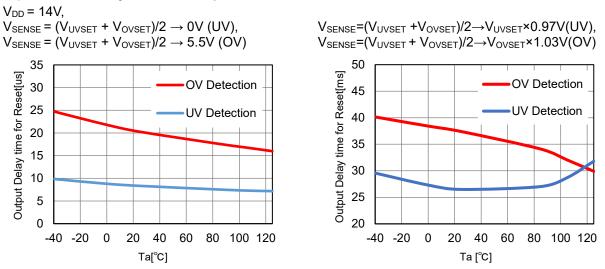








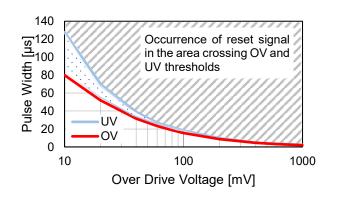
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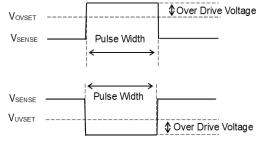


12) Detection Delay Time vs. Temperature

13) SENSE Pulse Width vs. Over Drive Voltage

 $V_{DD} = 14V$, $V_{SENSE} = (V_{UVSET}+V_{OVSET})/2 \rightarrow (V_{UVSET} - Over Drive Voltage) (UV)$, $V_{SENSE} = (V_{UVSET}+V_{OVSET})/2 \rightarrow (V_{OVSET} + Over Drive Voltage) (OV)$





POWER DISSIPATION

HSOP-18

PD-HSOP-18-(125150)-JE-B

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

ltem	Measurement Conditions			
Environment Mounting on Board (Wind Velocity = 0 m/s)				
Board Material Glass Cloth Epoxy Plastic (Four-Layer Board)				
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm			
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square			
Through-holes	φ 0.3 mm × 21 pcs			

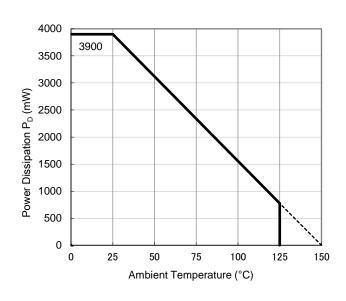
Measurement Result

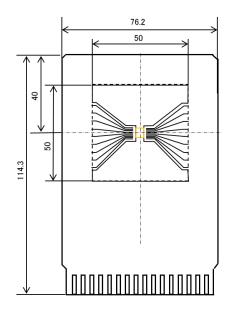
(Ta = 25°C, Tjmax = 150°C)

Item	Measurement Result
Power Dissipation	3900 mW
Thermal Resistance (θja)	θja = 32°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 8°C/W

 $\boldsymbol{\theta} ja:$ Junction-to-Ambient Thermal Resistance

wjt: Junction-to-Top Thermal Characterization Parameter





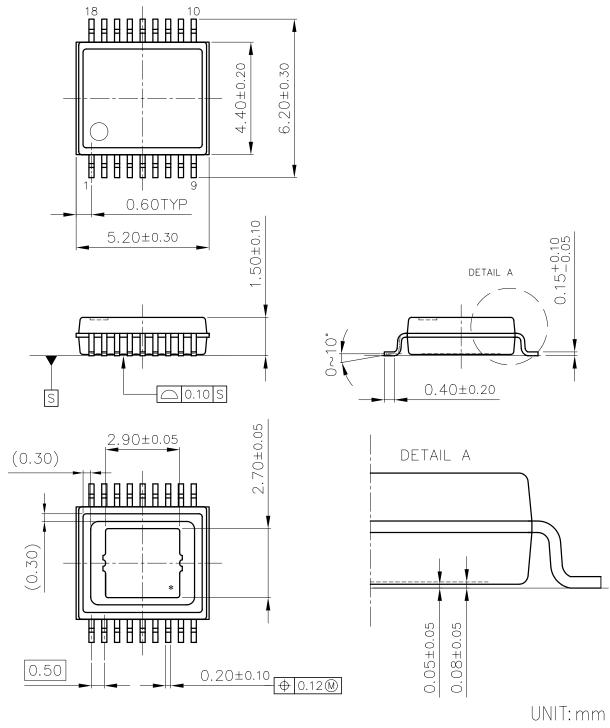
Power Dissipation vs. Ambient Temperature

Measurement Board Pattern

PACKAGE DIMENSIONS

HSOP-18

DM-HSOP-18-JE-B





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